ATIC12 (12-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

SPECIFICATION

VER. 1.2

General

The ATIC12 is 12-Channel capacitive sensor with auto sensitivity calibration. And the supply voltage range is from 3.0 to 5.0V.

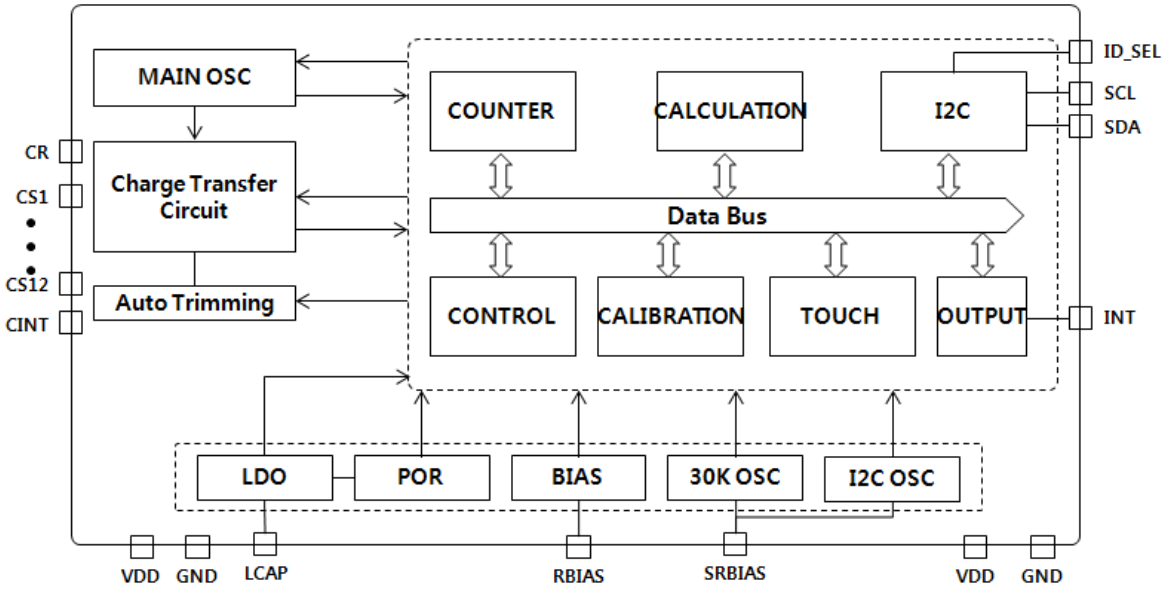
The result of touch sensing can be checked by the I^2C serial interface. I2C interface might be useful when the MCU IO or connector resource is not enough in the application.

The ATIC12 has the ID_SEL.
The ID_SEL is Chip ID selection input pin.

Feature

- 12-Channel capacitive sensor with auto sensitivity calibration
- I2C serial interface
- Selectable output operation mode (Single output / Multi output)
- Adjustable 32 steps sensitivity
- Low current consumption
- Embedded common and normal noise elimination circuit
- RoHS compliant 28 QFN / 28 SSOP packages
- Moisture sensitivity level 3 (MSL3)
- Typical current consumption 320 uA (@3.0V, R_B 510K Ohm)
- Sleep mode to reduce the current consumption 60uA (@3.0V, R_{SB} 2M Ohm)
- Typical current consumption 460 uA (@5.0V, R_B 510K Ohm)
- Sleep mode to reduce the current consumption 80uA (@5.0V, R_{SB} 2M Ohm)

Block Diagram



Application

- Home appliances (TV, Monitor keypads)
- Membrane switch replacement
- Sealed control panels, keypads
- Touch screen replacement application Home application

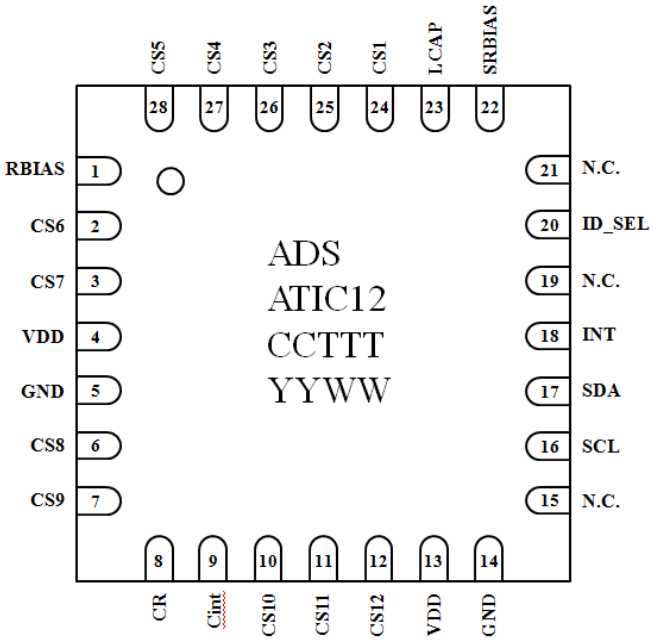
Ordering Information

Part No.	Package
ATIC12-QL	28 QFN
ATIC12-SL	28 SSOP

Content

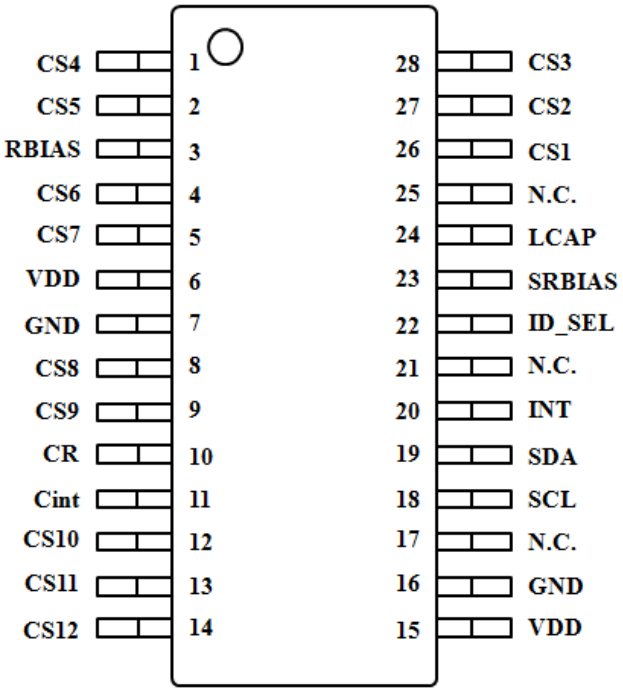
1 Pin Configuration

1.1 28 QFN Package



[28-QFN]

1.2 28 SSOP Package



[28 SSOP]

2 Pin Description

VDD, GND
Supply voltage and ground pin.

CR
Radio frequency Noise Detection pin. Normally, R.N.D pin does not connect to anywhere.
But, in radio frequency noise environment, this pin must form a pattern line on PCB.

CS1 ~ CS12
Capacitive sensor input pins.

LCAP
Internal LDO output port.

SCL, SDA
SCL is I^2C clock input pin and SDA is I^2C data input-output pin. These ports have internal pull-up resistor.
In case of not use, this pin must be not connected to any circuitry.

INT
Touch sensing interrupt output pin. This port has internal pull-up resistor.

ID_SEL
I2C Address selection input.

RBIAS
Internal bias adjust input. Normally 510K-ohm resistor is connected between this port and ground.

SRBIAS
Stand-by internal bias adjust input. Normally 2M-ohm resistor is connected between this port and ground.

Cint
Integration Capacitor.

2.1 Pin Map – 28 QFN Package

Pin Number	Name	I/O	Description	Protection
1	RBIAS	Analog I/O	Internal bias adjust input	VDD/GND
2	CS6	Analog I/O	CS6 Channel capacitive sensor input	VDD/GND
3	CS7	Analog I/O	CS7 Channel capacitive sensor input	VDD/GND
4	VDD	Power	Power Supply (3.0V ~ 5.5V)	GND
5	GND	Ground	Ground	VDD
6	CS8	Analog I/O	CS8 Channel capacitive sensor input	VDD/GND
7	CS9	Analog I/O	CS9 Channel capacitive sensor input	VDD/GND
8	CR	Analog I/O	Reference Channel capacitive sensor input	VDD/GND
9	Cint	Analog I/O	Integration Capacitor	VDD/GND
10	CS10	Analog I/O	CS10 Channel capacitive sensor input	VDD/GND
11	CS11	Analog I/O	CS11 Channel capacitive sensor input	VDD/GND
12	CS12	Analog I/O	CS12 Channel capacitive sensor input	VDD/GND
13	VDD	Analog I/O	Power Supply (3.0V ~ 5.5V)	GND
14	GND	Ground	Ground	VDD
15	N.C.	-	No connection	-
16	SCL	Digital I/O	I2C Clock input	VDD/GND
17	SDA	Digital I/O	I2C Data (Open drain)	VDD/GND
18	INT	Digital Out	Interrupt Output (Open drain)	VDD/GND
19	N.C.	-	No connection	-
20	ID_SEL	Digital I/O	I2C Address Selection	VDD/GND
21	N.C.	-	No connection	-
22	SRBIAS	Analog I/O	Stand-by mode internal bias input	VDD/GND
23	LCAP	Analog I/O	Internal LDO Output	VDD/GND
24	CS1	Analog I/O	CS1 Channel capacitive sensor input	VDD/GND
25	CS2	Analog I/O	CS2 Channel capacitive sensor input	VDD/GND
26	CS3	Analog I/O	CS3 Channel capacitive sensor input	VDD/GND
27	CS4	Analog I/O	CS4 Channel capacitive sensor input	VDD/GND
28	CS5	Analog I/O	CS5 Channel capacitive sensor input	VDD/GND

2.2 Pin Map – 28 SSOP Package

Pin Number	Name	I/O	Description	Protection
1	CS4	Analog I/O	CS4 Channel capacitive sensor input	VDD/GND
2	CS5	Analog I/O	CS5 Channel capacitive sensor input	VDD/GND
3	RBIAS	Analog I/O	Internal bias adjust input	VDD/GND
4	CS6	Analog I/O	CS6 Channel capacitive sensor input	VDD/GND
5	CS7	Analog I/O	CS7 Channel capacitive sensor input	VDD/GND
6	VDD	Power	Power Supply (3.0V ~ 5.5V)	GND
7	GND	Ground	Ground	VDD
8	CS8	Analog I/O	CS8 Channel capacitive sensor input	VDD/GND
9	CS9	Analog I/O	CS9 Channel capacitive sensor input	VDD/GND
10	CR	Analog I/O	Reference Channel capacitive sensor input	VDD/GND
11	Cint	Analog I/O	Integration Capacitor	VDD/GND
12	CS10	Analog I/O	CS10 Channel capacitive sensor input	VDD/GND
13	CS11	Analog I/O	CS11 Channel capacitive sensor input	VDD/GND
14	CS12	Analog I/O	CS12 Channel capacitive sensor input	VDD/GND
15	VDD	Analog I/O	Power Supply (3.0V ~ 5.5V)	GND
16	GND	Ground	Ground	VDD
17	N.C.	-	No connection	-
18	SCL	Digital I/O	I2C Clock input	VDD/GND
19	SDA	Digital I/O	I2C Data (Open drain)	VDD/GND
20	INT	Digital Out	Interrupt Output (Open drain)	VDD/GND
21	N.C.	-	No connection	-
22	ID_SEL	Digital I/O	I2C Address Selection	VDD/GND
23	SRBIAS	Analog I/O	Stand-by mode internal bias input	VDD/GND
24	LCAP	Analog I/O	Internal LDO Output	VDD/GND
25	N.C.	-	No connection	-
26	CS1	Analog I/O	CS1 Channel capacitive sensor input	VDD/GND
27	CS2	Analog I/O	CS2 Channel capacitive sensor input	VDD/GND
28	CS3	Analog I/O	CS3 Channel capacitive sensor input	VDD/GND

3 Absolute Maximum Rating

Battery supply voltage	5.5V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	-50 ~ 150℃
Operating Temperature	-20 ~ 75℃
Junction Temperature	150℃

Note : Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Max	Reference
H.B.M	Pos / Neg	8000 V	VDD
		8000 V	VSS
		7500 V	P to P
M.M	Pos / Neg	400 V	VDD
		450 V	VSS
		500 V	P to P
C.D.M	-	800 V	Field Induced Charge

4.2 Latch-up Characteristics

Mode	Polarity	Max	Reference
I Test	Positive	100 mA	JESD78A
	Negative	-100 mA	
V supply over 5.5V	Positive	8.25 V	

5 Electrical Characteristics

▪ V_{DD}=3.3V, Typical system frequency (Unless otherwise noted), T_A = 25℃

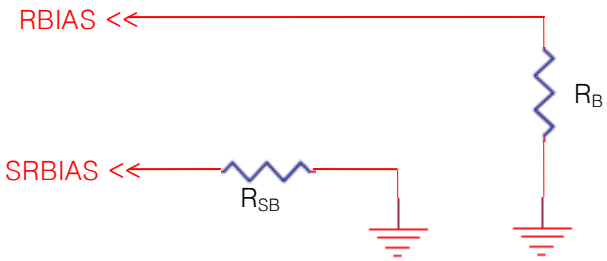
Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Power supply requirement and current consumption						
Operating voltage	V_{DD}		3.0		5.5	V
Current consumption	I_{DD}	V_{DD}= 3.0V, R_B=51K Ohm	-	320	-	uA
		V_{DD}= 3.0V, Sleep Mode state, R_{SB}=2M Ohm	-	60	-	
		V_{DD}= 5.0V, R_B=51K Ohm	-	460	-	
		V_{DD}= 5.0V, Sleep Mode state, R_{SB}=2M Ohm	-	80	-	
Reset and input level						
Internal Reset voltage	V_{DD_RST}	LCAP =1.8V	1.05	1.20	1.35	V
Input high level	VIH	$\lvert I_{IH} \rvert \leq +5\mu A$	V_{DD}*0.6		V_{DD}+0.3	V
Input low level	VIL	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		V_{DD}*0.3	V
Self calibration time after system reset	T_{CAL}	Normal calibration speed	-	300	-	msec
Touch sensing performance						
Minimum detective capacitance difference	ΔC_{MIN}		0.2	-	-	pF
Sense input capacitance range	C_S		-	-	36	pF
Output impedance (open drain)	Zo	$\Delta C > \Delta C_{MIN}$	-	12	-	Ω
		$\Delta C < \Delta C_{MIN}$	-	30M	-	
System performance						
Max. output current	I_{OUT}	Per unit drive output port	-	-	8.0	㎃
Sensitivity control			-	32	-	step
Max. I^2C SCL clock speed	f_{SCL_MAX}	Maximum internal I^2C clock	-	-	400	KHz

6 ATIC12 Implementation

6.1 Sensing Voltage setting

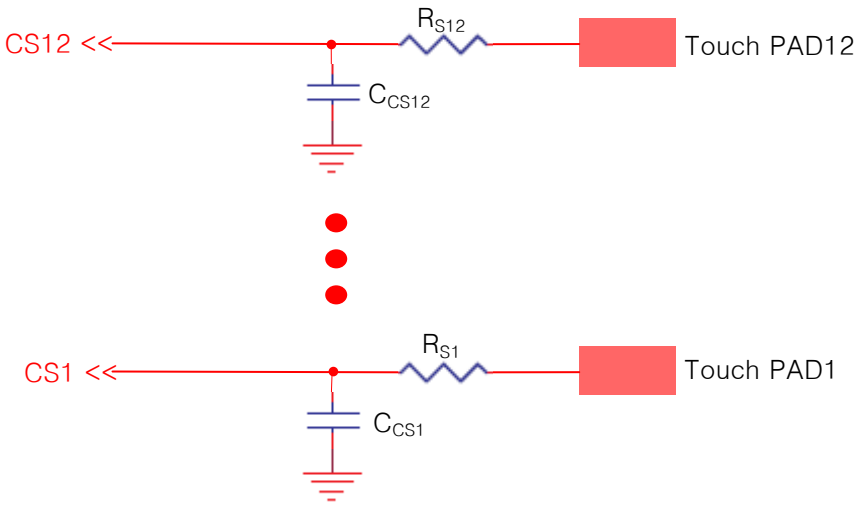
Sensing voltage of ATIC12 is set by VDD voltage after power-on reset.
If VDD voltage is 4.7V ~ 5.5V, sensing voltage is set 4.5V.
If VDD voltage is 3.0V ~ 4.7V, Sensing voltage is set 2.7V.
So, VDD voltage is not recommended between 4.6V from 4.8V.

6.2 RBIAS & SRBIAS implementation



The RBIAS is connecting to the resistor to decide the oscillator and internal bias current. The sensing frequency, internal clock frequency and current consumption are therefore able to be adjusted with R_B.
Normally, an R_B of 510K ohms is used. If user wants to use a different value of R_B, please contact AD Semiconductors.
The R_{SB} should be connected as above figure when the ATIC12 operates in SLEEP Mode to save the current consumption. In this case, the consumption depends on the R_{SB} and R_B resistors.

6.3 CS Implementation

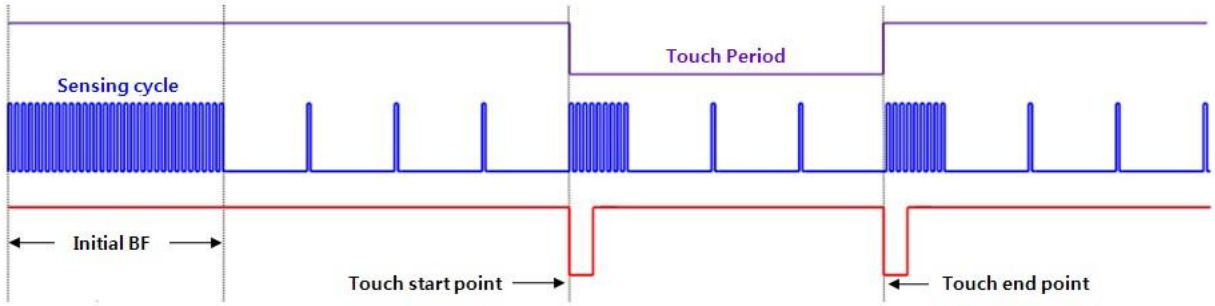


The ATIC12 has basically 32 steps sensitivity, which is available to control with internal register by I2C interface. The parallel capacitor C_{CS1} is added to CS1 and C_{CS12} to CS12 to adjust sensitivity. The sensitivity will

be increased when smaller value of C_{CS} is used. It could be useful in case detail sensitivity mediation is required. The internal touch decision process of each channel is separated from each other. The twelve channel touch key board application can therefore be designed by using only one ATIC12 without coupling problem. The R_S is serial connection resistor to avoid mal-function from external surge and ESD. (It might be optional.) From 100Ω to 1kΩ is recommended for RS. The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 ㎜ x 7 ㎜). The connection line of CS1 ~ CS12 to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line. The unused CS channel must be disabled with the channel reset[1] registers.

6.4 INT (Interrupt output) Implementation

An INT pin is for the touch sensing interrupt output. The interrupt pulse is generated only during short period of every each channel touch start point and touch end point. Interrupt pulse has logical low level. INT has NMOS open drain structure.



6.5 CINT implementation

In the operation of the ATIC12, it is necessary to integrate the sensing voltage. Thus, an external capacitor CINT is required for such operation.
If noise affects CINT capacitor, it can cause abnormal operation. Therefore, CINT Capacitor must be designed to minimize the effects of noise.

6.6 LCAP implementation

The ATIC12 has internal Regulator(LDO) for digital block operation. It is recommended that an external capacitor (LCAP) be connected for stable operation of the LDO. The position of LCAP should be as close as possible to the ATIC12 IC. LCAP, LACP capacitors and lines require a ground shield design to avoid being affected by a noise.

6.7 SCL, SDA implementation

SCL is I^2C clock input and SDA is I^2C data input-output. Maximum supported I^2C clock frequency is 4MHz. SDA has NMOS open drain structure. For more details refer to 'Chapter 10. I^2C Interface'.

[1] Refer to the chapter 11.2.5. Channel reset register.

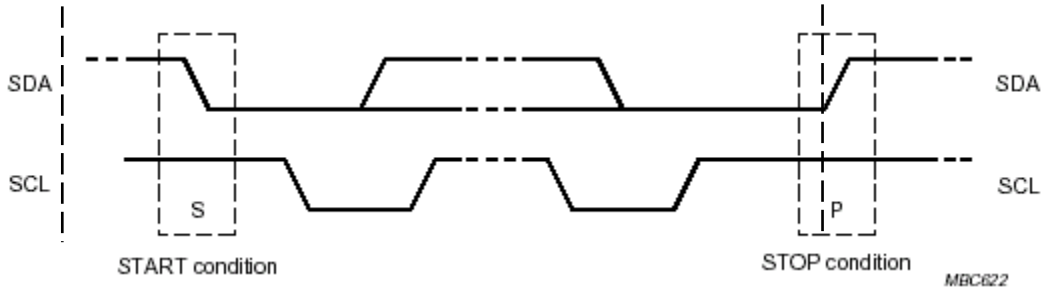
7 I²C Interface

7.1 I²C Enable / Disable

If the SDA or SCL signal goes to low, I²C control block is enabled automatically. And if the SDA and SCL signal maintain high during about 4 us, I²C control block is disabled automatically also.

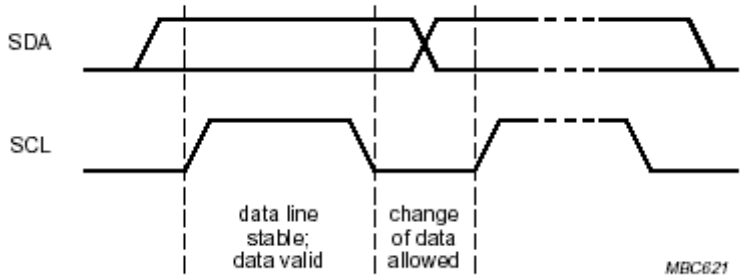
7.2 Start & stop condition

- Start Condition (S)
- Stop Condition (P)
- Repeated Start (Sr)



7.3 Data validity

The SDA should be stable when the SCL is high and the SDA can be changed when the SCL is low.

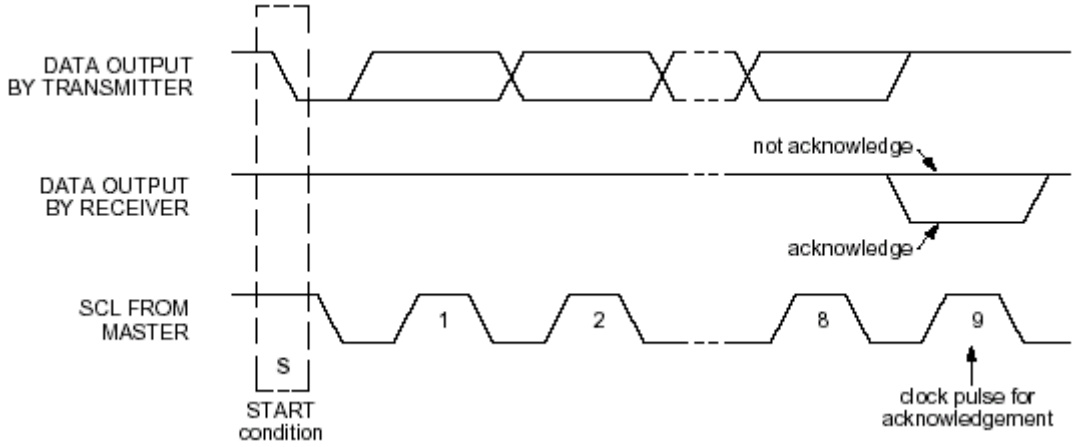


7.4 Byte format

The byte structure is composed with 8Bit data and an acknowledge signal.

7.5 Acknowledge

It is a check bit whether the receiver gets the data from the transmitter without error or not. The receiver will write **'0'** when it received the data successfully and **'1'** if not.



7.6 First byte

7.6.1 Slave address

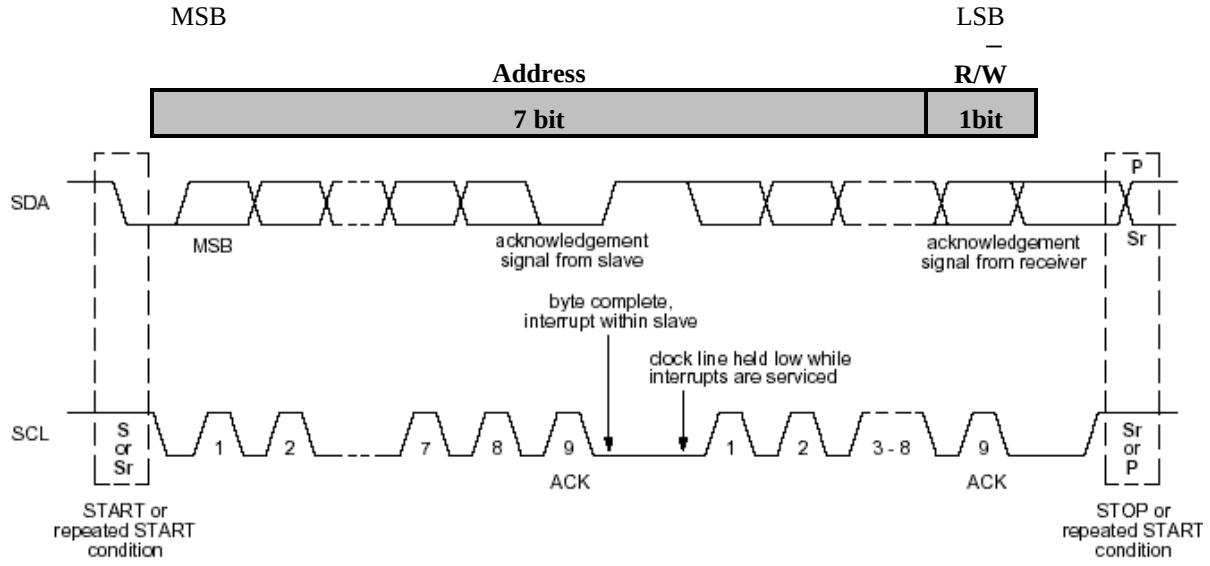
It is the first byte from the start condition. It is used to access the slave device.

ATIC12 Chip Address : 7bit

ID_SEL	Address
GND	0xD0
VDD	0xF0

7.6.2 R/$\overline{W}$

The direction of data is decided by the bit and it follows the address data.

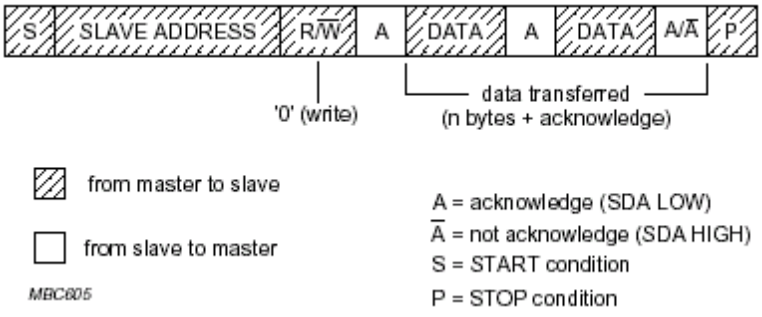


7.7 Transferring data

7.7.1 Write operation

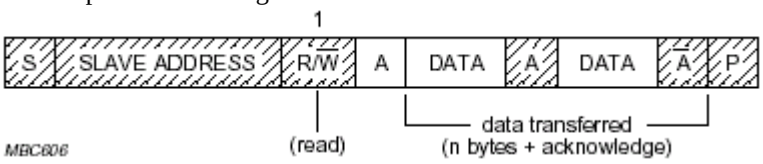
The byte sequence is as follows:

1. The first byte gives the device address plus the direction bit (R/W = 0).
2. The second byte contains the internal address of the first register to be accessed.
3. The next byte is written in the internal register. Following bytes are written in successive internal registers.
4. The transfer lasts until stop conditions are encountered.
5. The ATIC12 acknowledges every byte transfer.

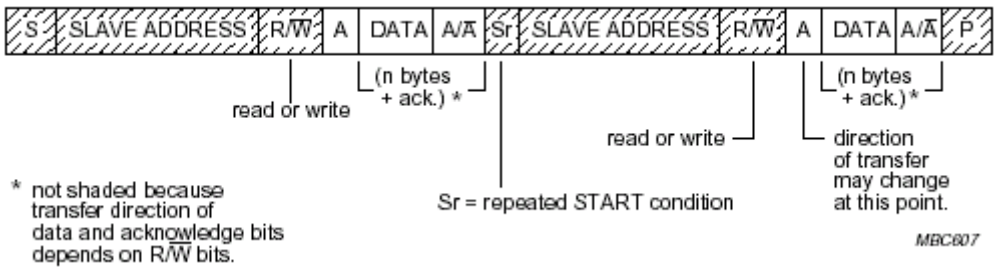


7.7.2 Read operation

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial address.



7.7.3 Read/Write Operation



7.8 I²C write and read operations in normal mode

The following figure represents the I²C normal mode write and read registers.

☞ Write register 0x00 to 0x01 with data AA and BB

Start	Device Address 0xD0	ACK	Register Address 0x00	ACK	Data AA	ACK	Data BB	ACK	Stop

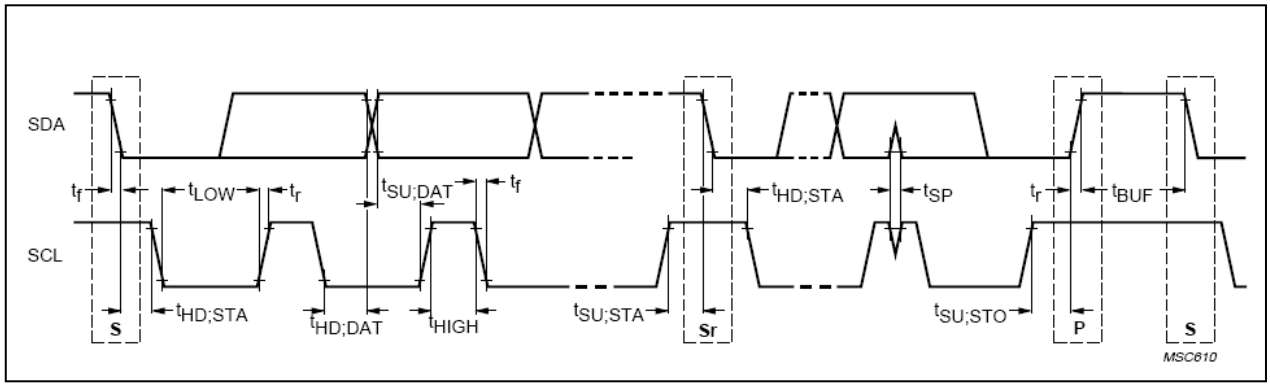
Read register 0x00 and 0x01

Start	Device Address 0xD0	ACK	Register Address 0x00	ACK	Stop

Start	Device Address 0xD1	ACK	Data Read AA	ACK	Data Read BB	$\overline{\text{ACK}}$	Stop

From Master to Slave From Slave to Master

7.9 I²C timing diagram



PARAMETER	SYMBOL	100kbps		400kbps		UNIT
		MIN.	MAX.	MIN.	MAX.	
Hold time (repeated)START condition.	tHD;STA	4.0	-	0.6	-	us
LOW period of the SCL clock	tLOW	4.7	-	1.3	-	us
HIGH period of the SCL clock	tHIGH	4.0	-	0.6	-	us
Set-up time for a repeated START condition	tSU;STA	4.7	-	0.6	-	us
Data hold time	tHD;DAT	1.0	-	-	-	us
Data set-up time	tSU;DAT	250	-	100	-	ns
Rise time of both SDA and SCL signals	tr	-	1000	20	300	ns
Fall time of both SDA and SCL signals	tf	-	300	20	300	ns
Set-up time for STOP condition	tSU;STO	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	tBUF	4.7	-	1.3	-	us
Noise margin at the LOW level for each connected device	VnL	0.1VDD	-	0.1VDD	-	V
Noise margin at the HIGH level for each connected device	VnH	0.2VDD	-	0.2VDD	-	V
Input Low level				0	V_{DD}*0.2	V
Input High level				V_{DD}*0.8	V_{DD}	V

8 ATIC12 control register list

◂ Note 1 : The unused bits (defined as reserved) in I²C registers must be kept to reset value.
◂ Note 2 : The empty bits (defined as '-') in I2C register are zero at read operation. So the empty bits are recommended as zero at write operation.

8.1 I²C Register Map

Name	Add. (Hex.)	Reset Value (Bin.)	Bit name of each bytes							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Sensitivity1	02	---0 0111	-	-	-	Sensitivity_CS01				
Sensitivity2	03	---0 0111	-	-	-	Sensitivity_CS02				
Sensitivity3	04	---0 0111	-	-	-	Sensitivity_CS03				
Sensitivity4	05	---0 0111	-	-	-	Sensitivity_CS04				
Sensitivity5	06	---0 0111	-	-	-	Sensitivity_CS05				
Sensitivity6	07	---0 0111	-	-	-	Sensitivity_CS06				
Sensitivity7	08	---0 0111	-	-	-	Sensitivity_CS07				
Sensitivity8	09	---0 0111	-	-	-	Sensitivity_CS08				
Sensitivity9	0A	---0 0111	-	-	-	Sensitivity_CS09				
Sensitivity10	0B	---0 0111	-	-	-	Sensitivity_CS10				
Sensitivity11	0C	---0 0111	-	-	-	Sensitivity_CS11				
Sensitivity12	0D	---0 0111	-	-	-	Sensitivity_CS12				
CTRL1	0E	0000 0011	BFMode	FTC		SingleMode	-	RTC		
CTRL2	0F	-001 0000	-	CDisTimeOpt	CSImpSel	1	SWReset	Sleep	FastRespMode	FastRespEn
Output1	10	Read Only	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
Output2	11	Read Only	-	-	-	-	OUT12	OUT11	OUT10	OUT9
Channel Reset 1	12	0000 0000	CHRst_8	CHRst_7	CHRst_6	CHRst_5	CHRst_4	CHRst_3	CHRst_2	CHRst_1
Channel Reset 2	13	---- 0000	-	-	-	-	CHRst_12	CHRst_11	CHRst_10	CHRst_9
Calibration Hold 1	14	0000 0000	CalHold_8	CalHold_7	CalHold_6	CalHold_5	CalHold_4	CalHold_3	CalHold_2	CalHold_1
Calibration Hold 2	15	---- 0000	-	-	-	-	CalHold_12	CalHold_11	CalHold_10	CalHold_9
Data Reading CH	20	---r 0000	-	-	-	RDDoneFlag	CS_Sel			
Ref. Data LSB	21	Read Only	SenseData[7:0]							
Ref. Data MSB	22	Read Only	SenseData[15:8]							
Sen. Data LSB	23	Read Only	RefData[7:0]							
Sen. Data MSB	24	Read Only	RefData[15:0]							
CS Sense Count LSB	25	Read Only	CSSenseCount[7:0]							
CS Sense Count MSB	26	Read Only	CSSenseCount[15:8]							
Error Percent	29	0010 ----	ErrModeOpt	ErrModeDisable	ErrPcntOpt		-	-	-	
CR Cal. Speed	2A	-100 -011	-	CRDnCalOpt			-	CRUpCalOpt		
CS Cal. Speed	2B	-100 -011	-	CSDnCalOpt			-	CSUpCalOpt		
Idle Time Control	2C	--00 ----	-	-	SleepTimeOpt		FastCalMode	FastBSOpt		FastBSEn

Name	Add. (Hex.)	Reset Value (Bin.)	Bit name of each bytes							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CS1 Cap. Control	31	--10 0000	-	-	CAP_SEL_CS1					
CS2 Cap. Control	32	--10 0000	-	-	CAP_SEL_CS2					
CS3 Cap. Control	33	--10 0000	-	-	CAP_SEL_CS3					
CS4 Cap. Control	34	--10 0000	-	-	CAP_SEL_CS4					
CS5 Cap. Control	35	--10 0000	-	-	CAP_SEL_CS5					
CS6 Cap. Control	36	--10 0000	-	-	CAP_SEL_CS6					
CS7 Cap. Control	37	--10 0000	-	-	CAP_SEL_CS7					
CS8 Cap. Control	38	--10 0000	-	-	CAP_SEL_CS8					
CS9 Cap. Control	39	--10 0000	-	-	CAP_SEL_CS9					
CS10 Cap. Control	3A	--10 0000	-	-	CAP_SEL_CS10					
CS11 Cap. Control	3B	--10 0000	-	-	CAP_SEL_CS11					
CS12 Cap. Control	3C	--10 0000	-	-	CAP_SEL_CS12					
Voltage Threshold Control 1	3D	---0 1101	-	-	-	AUTO_VCON				
Voltage Threshold Control 2	3E	---0 0101	-	-	-	INT_VCON				

8.2 Details

8.2.1 Sensitivity Control Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h ~ 0Dh	Sensitivity1 ~ Sensitivity12	-	-	-	Sensitivity_CS01 ~ Sensitivity_CS12				

Description

Set the sensitivity of each channel.

Bit name	Reset value	Function
Sesitivity_CSxx	00111	Each channel Sensitivity = Sensitivity_CSxx[4:0] * 0.1%

8.2.2 System Control Register 1

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Eh	CTRL1	BFMode	FTC		Single Mode	-	RTC		

Description

The calibration speed just after power on reset is very high during the time which is defined by FTC[1:0] to have a good adoption against unstable external environment.

Bit name	Reset value	Function
BFMode	0	Sensing mode selection. * '0' : Auto alternate mode – BF/BS(Sleep) * '1' : BF Mode Only
FTC	00	Set the initial BF Sensing Time. * 00 : 1-Period(18ms) * 278 = about 5 s, 01 : 1-Period(18ms) * 556 = about 10 s * 10 : 1-Period(18ms) * 834 = about 15 s, 11 : 1-Period(18ms) * 1023 = about 18.4 s
SingleMode	0	Determines output Mode. * '0' : Multi-Output Mode * '1' : Single-Output Mode
RTC	011	Response Time Control Response period = RTC[2:0] + 1

8.2.3 System Control Register 2

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Fh	CTRL2	-	CDisTimeOpt	CSImpSel	1	SWReset	Sleep	FastRespMode	FastRespEn

Description

All the digital blocks except analog and I2C block are reset when 'SWReset' is set. The 'Sleep' function allows getting very low current consumption when it is set. But the response time will be longer than normal operation.

Bit name	Reset value	Function
CDisTimeOpt	0	The discharge time control register for the capacitor, Cint. * 0 : 1us * 1 : 1us + 61us
CSImpSel	0	Select Impedance of CS Line. (excluding Sensing time) * 0 : High Impedance * 1 : Low Impedance
SWReset	0	Software Reset * 0 : Disable Software Reset * 1 : Enable Software Reset
Sleep	0	Sleep Mode Enable * 0 : Disable Sleep Mode * 1 : Enable Sleep Mode
FastRespMode	0	Determining operation Mode when the 'FastRespEn' bis is set. * 0 : Continuous 3 times sensing. * 1 : Continuous 2 times sensing.
FastRespEn	0	Function to only continuous sensing of Touch detected channels. To shorten the response time. * 0 : Disable * 1 : Enable

8.2.4 Output Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	Output1	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
11h	Output2	-	-	-	-	OUT12	OUT11	OUT10	OUT9

Description

Output of each channel.

Bit name	Reset value	Function
OUT1 ~ OUT12	0	Output of each channel * 0 : No output * 1 : Output

8.2.5 Channel Reset Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
12h	Channel Reset1	CHRst_8	CHRst_7	CHRst_6	CHRst_5	CHRst_4	CHRst_3	CHRst_2	CHRst_1
13h	Channel Reset2	-	-	-	-	CHRst_12	CHRst_11	CHRst_10	CHRst_9

Description

The operation of each channel is independently available to control. A channel doesn't be worked and the calibration is reset when it is set.

Bit name	Reset value	Function
CHRst_1 ~ CHRst_12	0	0: Enable operation (sensing + calibration) 1: Reset operation (No sensing + reset calibration)

8.2.6 Calibration Hold Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
14h	Calibration Hold1	CalHold_8	CalHold_7	CalHold_6	CalHold_5	CalHold_4	CalHold_3	CalHold_2	CalHold_1
15h	Calibration Hold2	-	-	-	-	CalHold_12	CalHold_11	CalHold_10	CalHold_9

Description

The calibration of each channel is independently available to control. Each channel is working even if a bit is set.

Bit name	Reset value	Function
CalHold1 ~ CalHold12	0	* 0: Enable reference calibration (sensing + calibration) * 1: Disable reference calibration (sensing + No calibration)

8.2.7 Data Read Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h	Data Reading CH	-	-	-	RDDoneFlag	CS_Sel			
21H	Ref. Data LSB	SenseData[7:0]							
22H	Ref. Data MSB	SenseData[15:8]							
23H	Sen. Data LSB	RefData[7:0]							
24H	Sen. Data MSB	RefData[15:0]							
25H	CS Sense Count LSB	CSSenseCount[7:0]							
26H	CS Sense Count MSB	CSSenseCount[15:8]							

Description

It monitors count data in the channel.

Bit name	Reset value	Function
RDDoneFlag	Read Only	Data Update Flag * 0 : No Updated * 1 : Updated
CS_Sel	0000	Selecting a channel to be read data * 0000 : CR Channel * 0001 ~ 1100 : CS1 ~ CS12 Channel
SenseData	Read Only	Current Data of the selected channel *CR channel – Sense Count * CS channel – Sense Percent
RefData	Read Only	Current Ref. Data of the selected channel * CR channel – Current Ref. Count * CS channel – Current Ref. Percent
CSSenseCount	Read Only	Display of the selected channel Sense Count

8.2.8 Error Percent Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
29h	Error Percent	ErrModeOpt	ErrModeDisable	ErrPcntOpt					

Description

To set the error mode options.

Bit name	Reset value	Function
ErrModeOpt	0	If Error Mode, Touch behaves decision * 0 : Touch Integral number = Set touch Integral number + Error Count(Dummy) * 1 : Touch Integral number = Set touch Integral number + Error Count(Each channel)
ErrModeDisable	0	Error Mode Disable * 0 : Error Mode Enable * 1 : Error Mode Disable
ErrPcntOpt	10	ErrPcntOpt : CR Channel Error Percent Option * 00 : 0.4% / 01 : 0.6% / 10 : 0.8% / 11 : 1.0% * It exceeds Error Percent and 4 continuous cycle are Error Mode → Fast Calibration : 4/1(UP), 1/1(Down)

8.2.9 Calibration Speed Control Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ah	CR Cal. Speed	-	CRDnCalOpt			-	CRUpCalOpt		
2Bh	CS Cal. Speed	-	CSDnCalOpt			-	CSUpCalOpt		

Description

To set the auto calibration speed of channels.

Bit name	Reset value	Function
CRDnCalOpt	100	**Calibration speed Option of CR Channel - Down direction** * 000 : 1/1 * 001 : 1/2 * 010 : 1/4 * 011 : 1/8 *** 100 : 1/16(Reset)** * Others : 1/32
CRUpCalOpt	011	**Calibration speed Option of CR Channel - Up direction** * 000 : 1/1 * 001 : 1/2 * 010 : 1/4 *** 011 : 1/8(Reset)** * 100 : 1/16 * Others : 1/32
CSDnCalOpt	100	**Calibration speed Option of CR Channel - Down direction** * 000 : 1/1 * 001 : 1/2 * 010 : 1/4 * 011 : 1/8 *** 100 : 1/16(Reset)** * Others : 1/32
CSUpCalOpt	011	**Calibration speed Option of CR Channel - Up direction** * 000 : 1/1 * 001 : 1/2 * 010 : 1/4 *** 011 : 1/8(Reset)** * 100 : 1/16 * Others : 1/32

8.2.10 Sleep Time Control Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ch	Sleep Time Control	-		SleepTimeOpt		FastCalMode	FastBSOpt		FastBSEn

Description

Sleep Mode 에서의 주기를 결정한다.

Bit name	Reset value	Function
SleepTimeOpt	00	When Sleep mode, Sensing Cycle Select Option. * 00 : 200ms * 01 : 300ms * 10 : 400ms * 11 : 500ms
FastCalMode	1	To Select the condition to finish from Fast BS Calibration mode. * 0 : To finish from Fast BS Calibration mode after the set time. * 1 : To finish form Fast BS Calibration mode after the set time or touched.
FastBSOpt	00	Time Setting in Fast BS Calibration Mode * 00 : 1 minute * 01 : 2 minute * 10 : 3 minute * 11 : 4 minute
FastBSEn	1	Fast BS Calibration Mode Enable * 0 : Disable * 1 : Enable

8.2.11 Internal Capacitance Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
30h	CR Cap. Control	-	-	CAP_SEL_CR					
31h ~ 3Ch	CS1 Cap. Control ~ CS12 Cap. Control	-	-	CAP_SEL_CS1 ~ CAP_SEL_CS12					

Description

The internal capacitance is set as same as the total capacitance of CS channels after power-on reset.
And the internal capacitance can be changed by this register.

Bit name	Reset value	Function
CAP_SEL_CR	100000	**Internal Cap. value(CR Channel)is stored in this register.** * Internal Capacitance = CAP_SEL_CR[5:0] * 0.742pF
CAP_SEL_CS1 ~ CAP_SEL_CS12	100000	**Internal Cap. value(CS1 ~ CS12 Channel)is stored in this register.** * Internal Cap. Value = CAP_SEL_CR[5:0] * 0.742pF

8.2.12 Voltage Threshold Control Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Dh	Voltage Threshold Control 1	-	-	-	AUTO_VCON				
3Eh	Voltage Threshold Control 2	-	-	-	INT_VCON				

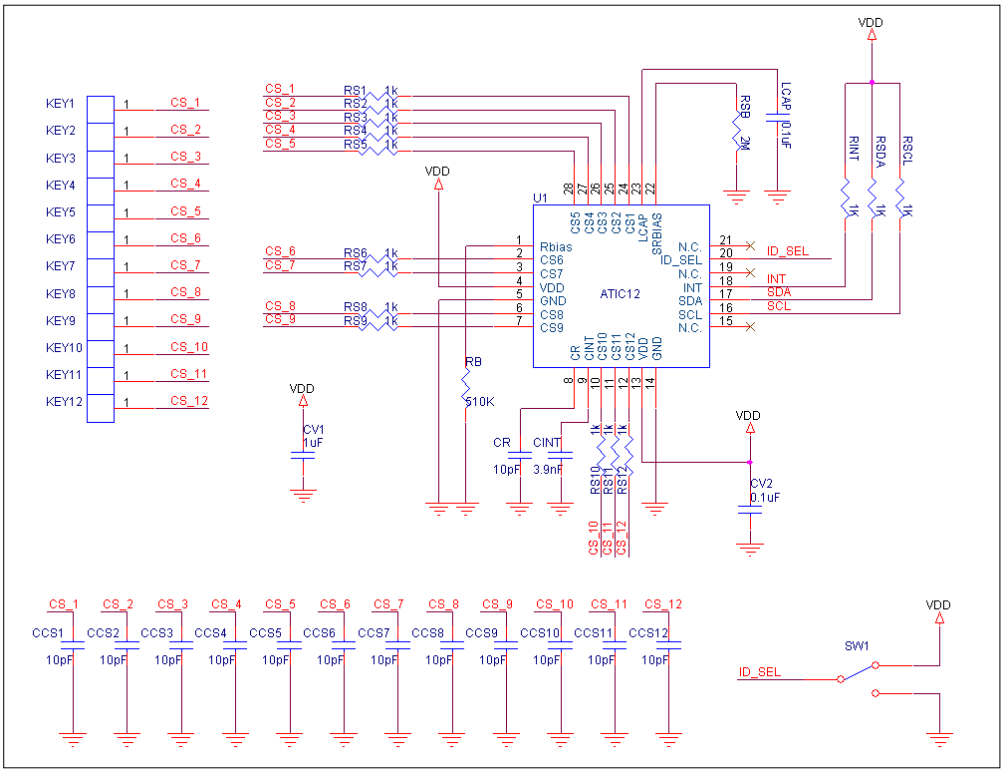
Description

It determines the reference voltage of the comparator.

Bit name	Reset value	Function
AUTO_VCON	01101	Voltage level to compare the CS Cap. and internal Cap. Voltage level corresponding to this value
INT_VCON	00101	Comparator reference voltage to comparison with Cin voltage (Vref) Voltage level corresponding to this value

9 Recommended Circuit Diagram

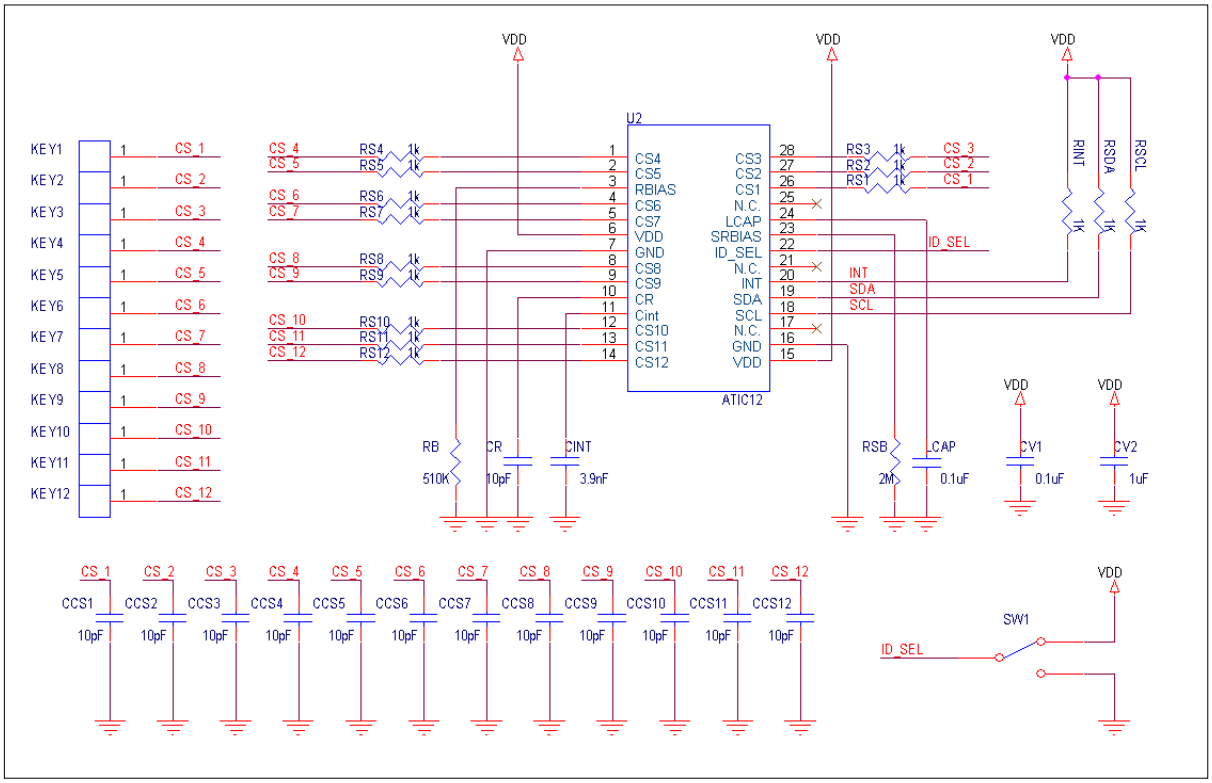
9.1 ATIC12 – 28 QFN



ATIC12 Application Example Circuit

- ✓ ATIC12 is reset by internal reset circuit. VDD voltage rising time should be shorter than 100msec for proper operation.
- ✓ Normally, R.N.D pin dose not connection to anywhere. But, in radio frequency noise environment, R.N.D pin must form a pattern line on PCB.
- ✓ The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- ✓ The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm.
- ✓ Parallel capacitor of CS pin could be useful in case detail sensitivity mediation is required such as for complementation sensitivity difference between channels.
- ✓ Serial connection resistor of CS pins may be used to avoid mal-function from external surge and ESD and the closer to IC(ATIC12), the stronger immunity against mal-function and ESD is.
- ✓ ATIC12 has a possibility to occur a jitter in the noisy environment. In this case, the BS Mode is switched to the BF Mode.
- ✓ The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from ATIC12.
- ✓ The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- ✓ The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.

9.2 ATIC12 – 28 SSOP



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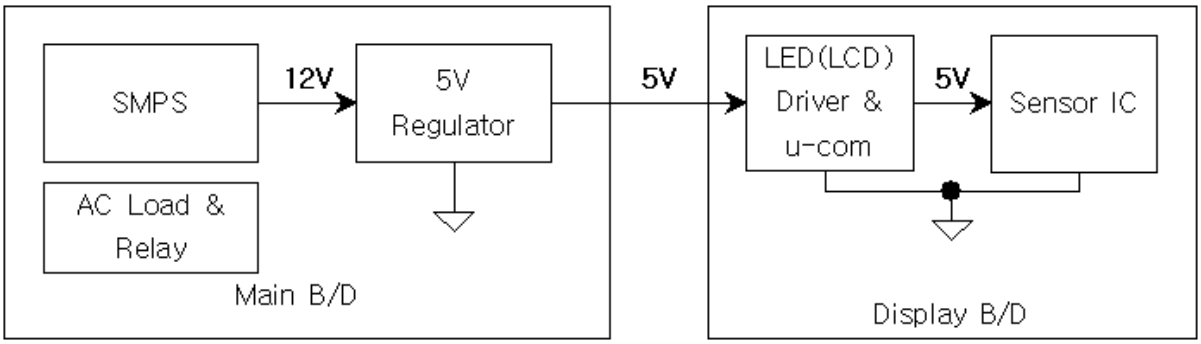
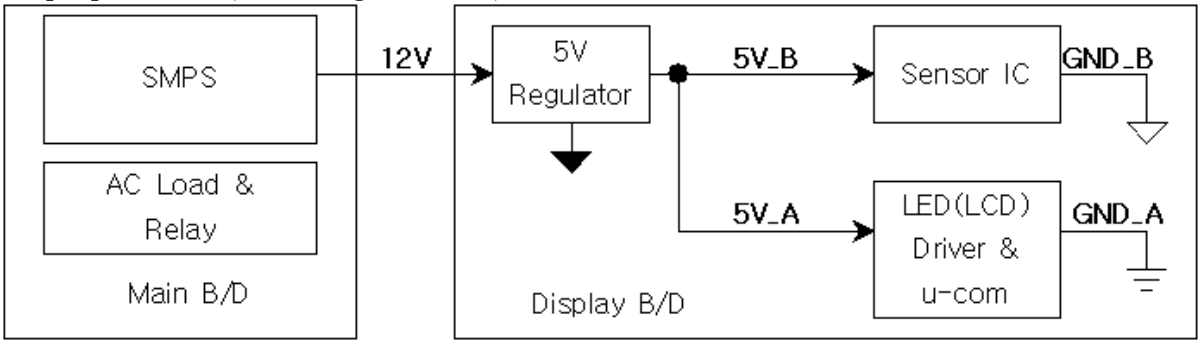
9.3 Example – Power Line Split Strategy PCB Layout

A. Not split power Line (Bad power line design)

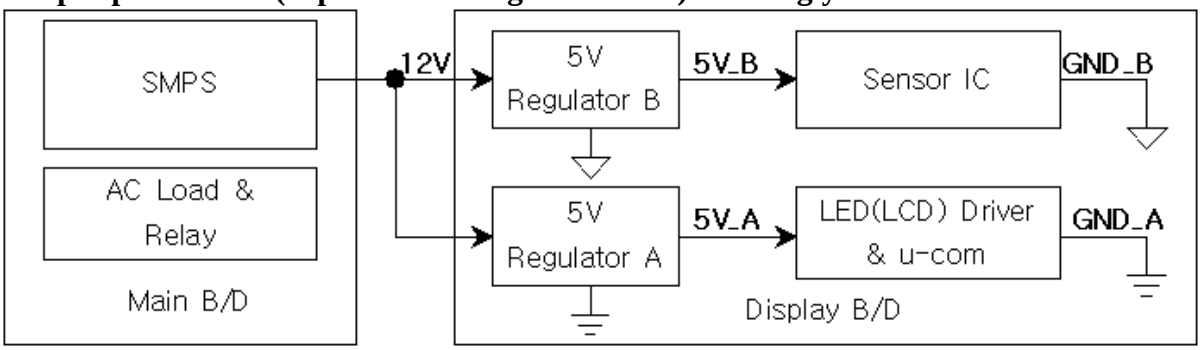


- ✓ The The noise that is generated by AC load or relay can be loaded at 5V power line.
- ✓ A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

B. Split power Line (One 5V regulator used) – Recommended

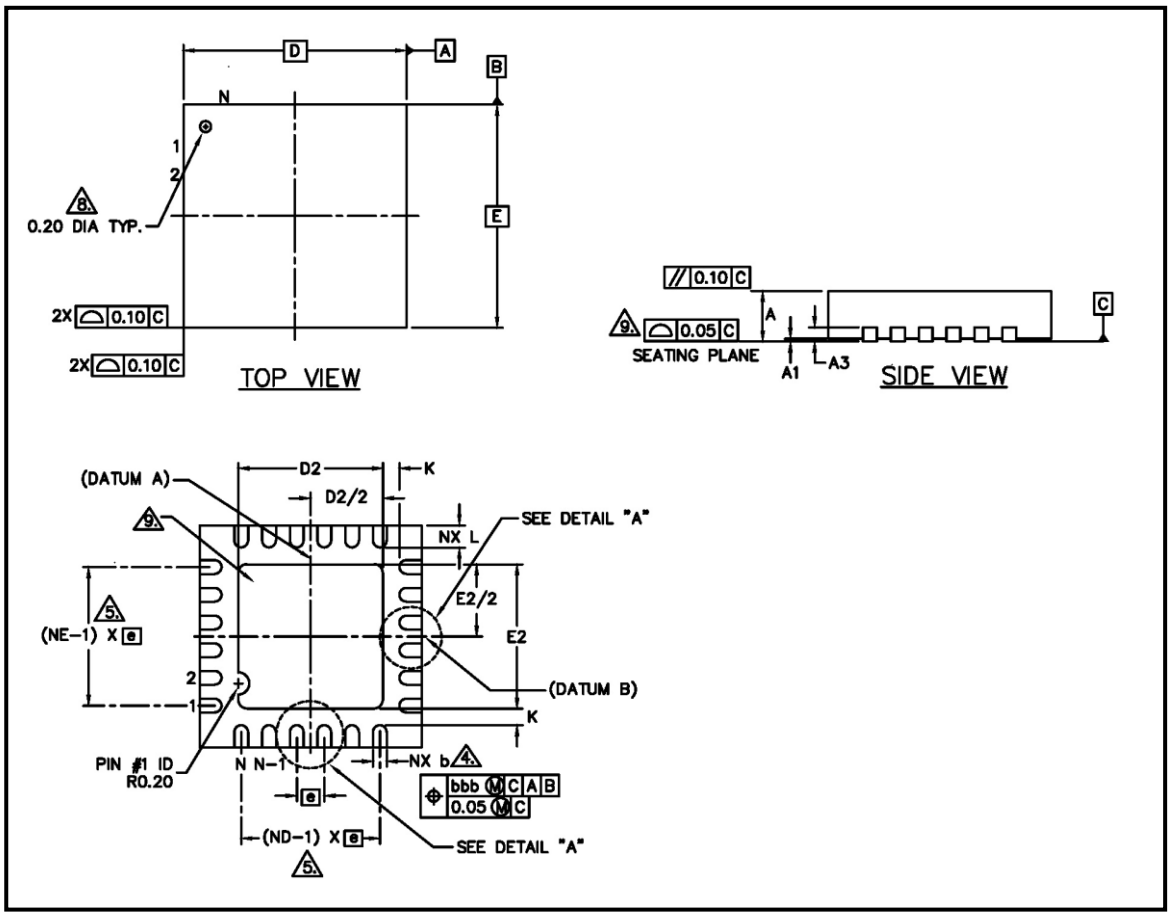


C. Split power Line (Separated 5V regulator used) – Strongly recommended



10 MECHANICAL DRAWING

10.1 Mechanical Drawing of ATIC12 - 28 QFN

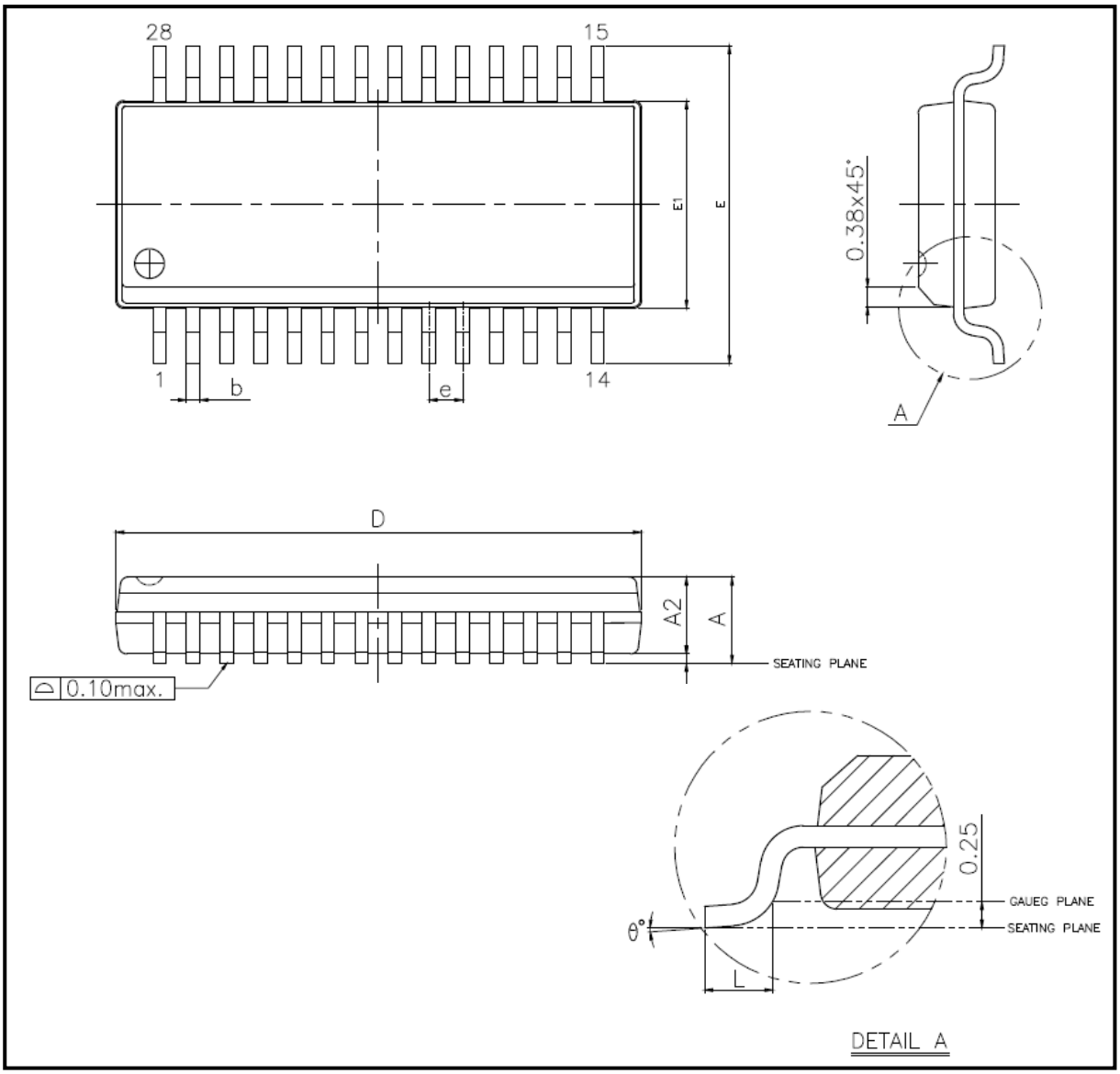


SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
A3		0.20 REF.		
θ	0	—	12	2
K		0.20 MIN.		
D		4.0 BSC		
E		4.0 BSC		
L1		0.15 mm MAX		11

SYMBOL	0.40mm LEAD PITCH VARIATION A			NOTE
	MIN.	NOM.	MAX.	
e		0.40 BSC		
N		28		3
ND		7		5
NE		7		5
L	0.35	0.40	0.45	11
b	0.15	0.20	0.25	4
D2	2.50	2.60	2.70	
E2	2.50	2.60	2.70	

NOTES :
1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220
11. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULLBACK (L1) MAYBE PRESENT
12. PULLBACK DESIGN OPTION IS FOR 0.50mm NOMINAL LANDLENGTH ONLY.

10.2 Mechanical Drawing of ATIC12 - 28 SSOP



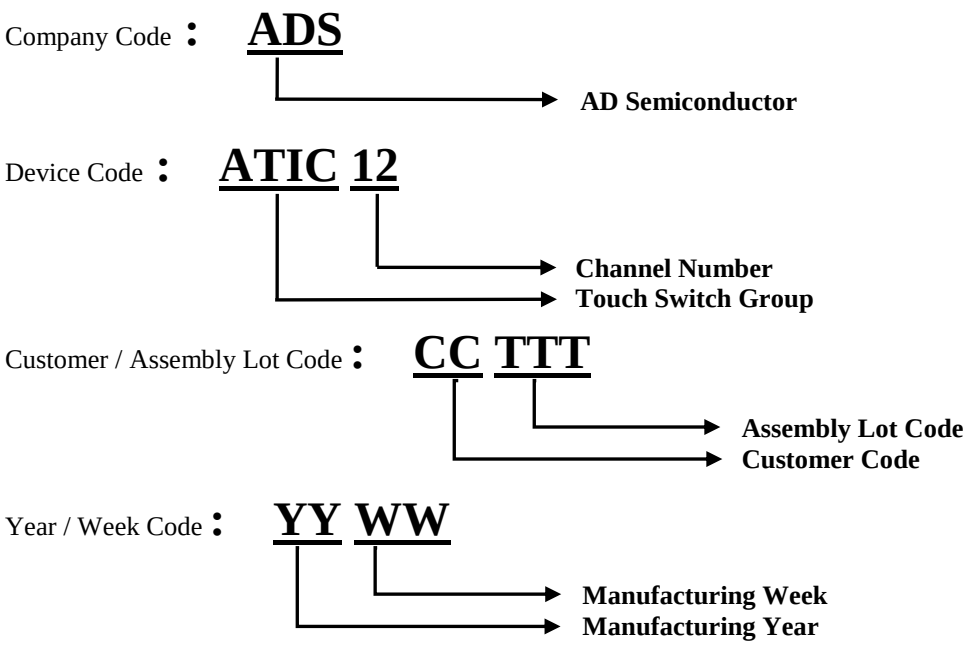
SYMBOLS	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
A2	–	1.50
b	0.20	0.30
D	9.80	10.00
E1	3.81	3.99
e	0.635 BASIC	
E	5.79	6.20
L	0.41	1.27
θ°	0	8

UNIT : MM

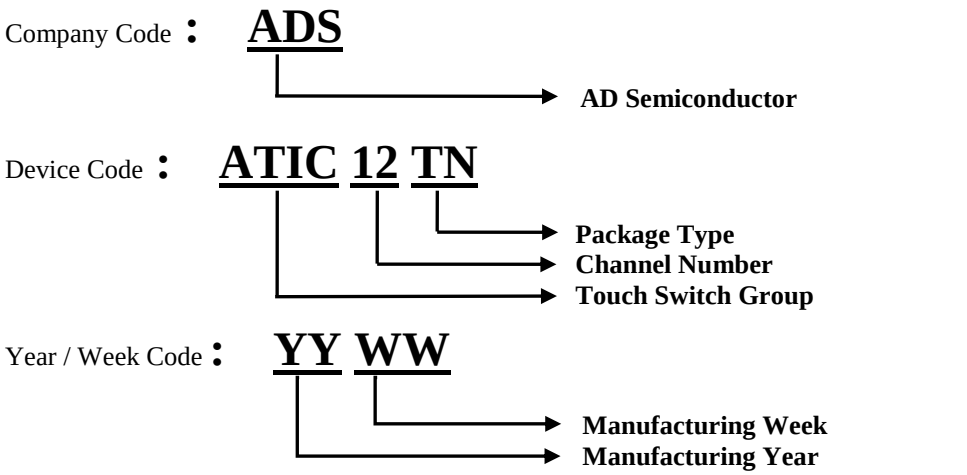
NOTES:
1. JEDEC OUTLINE : MO-137 AF
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (0.006in) PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm (0.010in) PER SIDE.

11 MARKING DESCRIPTION

11.1 Marking Description of ATIC12 – 28 QFN



11.2 Marking Description of ATIC12 – 28 SSOP



NOTES:

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